

What is claimed is:

1. An organic switching memory device, comprising:
 - a plurality of first electrode lines;
 - an organic memory layer formed on said plurality of first electrode lines, said organic memory layer having a voltage-current hysteresis characteristic;
 - a semiconductor diode layer stacked on said organic memory layer; and
 - a plurality of second electrode lines formed on said semiconductor diode layer, said plurality of second electrode lines being disposed in a direction so as to intersect said plurality of first electrode lines.
2. The organic switching memory device according to claim 1, wherein said semiconductor diode layer is a pn-junction diode layer.
3. The organic switching memory device according to claim 1, wherein said semiconductor diode layer is a Schottky diode layer.
4. A memory apparatus, comprising:
 - a organic switching memory device including:
 - a plurality of first electrode lines;
 - an organic memory layer formed on said plurality of first electrode lines, said organic memory layer having a voltage-current hysteresis characteristic;
 - a semiconductor diode layer stacked on said organic memory layer; and
 - a plurality of second electrode lines formed on said

semiconductor diode layer, said plurality of second electrode lines being disposed in a direction so as to intersect said plurality of first electrode lines,

a receiver section for receiving an address designation

5 signal, data and a write command signal, said address designation signal designating addresses which correspond to intersecting positions of said plurality of first electrode lines and said plurality of second electrode lines, and

a control section which writes the data to said organic

10 switching memory device on the basis of the address designation signal, in response to the write command signal.

5. The memory apparatus according to claim 4, wherein:

said receiver section receives a read command signal, and
said control section reads out data from said organic

15 switching memory device on the basis of said address designation signal, in response to said read command signal.